Nasa CR 65376

A Report

FINAL REPORT

FOR

PREMODULATION FILTERS

SCI PART NO. 1185001-1

CONTRACT NAS9-4393

[redacted]

TO

NASA

MANNED SPACEFLIGHT CENTER

HOUSTON, TEXAS

APRIL 1966

Space Craft, Inc.

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1.0 INTRODUCTION

The Pre-modulation Filters as designed by Space Craft Inc. consist of seven basic circuits as shown in the block diagram of figure 1. These filters employ a signal reconstruction technique. The use of this technique was dictated by the requirement for an isolated input to the filter and at the same time having the possibility of a nearly pure D.C. input signal. The method employed allows the filters to handle a D.C. signal with transformer coupling, and also provides very good noise rejection.

This report is devoted to giving the basic operation principles of each sub-circuit and its function in the overall circuit. Figure 2 is a detailed schematic diagram of the 800 Bit/sec pre-modulation filter.

2.0 CIRCUIT DESCRIPTION

2.1 Voltage Regulator

The specified output amplitude tolerances and operating voltage specifications require that internal regulation and filtering of the circuit operating voltages be provided. This is accomplished by the power regulator shown in figures 1 and 2. The regulator used is a Darlington connected series type regulator. CR2 is the internal voltage reference and Q2 acting as a comparator, and compares the feedback voltage to the reference to produce a control signal for the regulating devices, Q1 and Q23. Input filtering is used to minimize current feedback into the 28 vdc source and to aid the regulator in smoothing the input voltage. Diode CR1 furnishes reverse polarity protection and which with C1 produces a peak reading action that improves the rejection of ripple on the 28 vdc line.

2.2 DC to DC Inverter

To satisfy the requirement for a d.c. isolated input, isolated operating voltages are required for the input buffer circuit. These voltages are provided by a DC-DC converter consisting of a free-running multivibrator, transformer T1, and diodes CR13 and CR14. The multivibrator is basically standard in its design. Q3 and Q5 and diodes CR3 and CR4 form a standard emitter follower pull-up circuit to decrease the rise time of the circuit to acceptable limits. Diodes

CR8 and CR9 protect the base-emitter junctions, and together with resistors R52 and R53 aid in the self-starting ability of the multivibrator. A charge transfer circuit is incorporated to generate a negative voltage required by other circuitry. Both the charge transfer circuit and transformer T1 are driven by a push-pull method. This use of full wave rectifying techniques greatly reduces the filtering requirements of the inverter output voltages as well as reducing feedback to the regulated B+ lines. Resistor R6 and capacitor C5 provide isolation and filtering of the B+ line to the inverter circuit.

2.3 Input Buffer

The input buffer stage is a conventional high input impedance, unity gain, low output impedance amplifier. Resistor R14 is included to reduce voltage noise that appears when used with high impedance signal sources. With high source impedances noise is present due to stray capacitive coupling of high-frequency signal components back to the input line. Resistor R14 and stray capacitance at the base of Q7 also act as a filter against unwanted high-frequency input noise. Capacitor C14 is used to prevent high-frequency instability of the input buffer. Coupling capacitor C15 and transformer T2 form a differentiating circuit that provides fast voltage spikes used to trigger the toggled flip-flop, at the same time isolating the input-signal common from other commons in the system.

2.4 Toggled Flip-Flop

The toggled flip-flop is a fairly conventional complementary flip-flop. When power is applied to the pre-modulation filter, and no input signed is present, the flip-flop output will go to it's most negative state. Resistor R55 in parallel with the load resistance is the detirmining component in the inital state of the flip-flop. With R55 being smaller than R23, Q11 will receive a stronger initial forward biasing current than is possible for Q13, therefore Q11 will turn on bringing Q14 on with it. The regenerative action of the circuit then results in Q12 and Q14 turning off. The flip-flop will remain in this state until a positive voltage pulse is received from the lower section of the transformer T2 secondary winding through CR19. This pulse tends to turn off Q11 lowering it's collector voltage and causing Q13 to turn on. Regenerative action then quickly continues the transition bringing the output of the flip-flop positive. Transition time of the flip-flop is less than 100 nanoseconds in both directions. Because of the fast transition time of the flip-flop only very small current spikes are generated on the B+ line. Capacitor C17 is provided to absorb whatever current spikes are generated. Resistors R16 and R17 provide DC biasing on the secondary of transformer T2 to detirmine the minimum amplitude of the triggering pulses needed to trigger the toggled flip-flop. Very good signal to noise rejection is possible with this method since no signal below the preset level can trigger the flip-flop. Very good signal to noise rejection is possible with this method since no signal below the preset level can trigger the flip-flop. A signal to noise rejection ratio approaching unity is possible, however a ratio considerably less than unity was chosen in order to

ensure reliable operation. Diode CR18 provides temperature stability of the biasing point, and capacitor C16 filters out any AC components. Immunity to low frequency noise is provided by the differentiating action of C15 - T2.

2.5 Filter Circuits

The output of the flip-flop is fed into a 6th order active filter. The amplifiers used in each section are of standard design. Each is a unity gain, high input impedance, low output impedance circuit. Each section is of a 3rd order configuration. Components values for the filter were first calculated and then adjusted empirically on the headboard model to obtain optimum results with standard values. Once component values were determined for one frequency, direct frequency scaling was used to obtain other values for filters of other bit rates. The frequency response characteristics of the filter circuits is calculated to be of the Buttersworth-Thompson form, giving a compromise of the flatness of the Buttersworth and the linear time delay of the Bessel types. Close tolerance capacitors and resistors are necessary in the filter sections to eliminate the need for selecting components for the different bit-rate filters.

The output of the filters section is direct coupled to two output buffers which furnish the two specified output signals.

2.6 Output Buffers

The output No. 2 buffer is a standard "cascode doublett" unity gain amplifier. The output amplitude is determined by adjusting resistor

R45, and is one of the component selections necessary during the manufacturing process. Diode CR24 provides temperature compensation for V_{BE} drift. Short circuiting output No. 2 to ground will not cause the current drawn by this stage to increase above its normal operating maximum. Long term short circuits will not damage the circuit or alter its operation when the short is removed.

The output No. 1 buffer is a similar "cascode doublet" amplifier. Resistor R49, R50 and R51 allow the gain of this buffer to be adjusted. When the buffer input is at ground potential the output voltage is negative and is a function of amplifier gain and the supply voltage at the emitter of Q21. Therefore adjusting R49 will determine the negative output voltage whenever the input voltage goes to zero. Adjusting R48 determines the maximum positive voltage of the output signal. Resistors R48 and R49 are selected during the manufacturing process. Short circuit protection is similar to that of output No. 2 buffer with resistor R35 keeping the current through Q22 at a safe level whenever the input is below the emitter voltage of Q21.

3.0 CIRCUIT OPERATION SUMMARY

Special attention was given to eliminating ground-loop problems by providing seperate ground leads from the various circuits to the ground pin of the connector.

Some noise is fed into the output buffers via the supply voltages, and are present at the output. This noise apparently originates in both the inverter circuit and the toggled flip-flop circuit. Experiments with the breadboard indicate that lowering of the high frequency response of the output buffers would decrease this noise.

4.0 EXPLANATION OF DOCUMENTATION

Documentation for the pre-modulation filters is arranged for the most efficient production of the filters. Each bit-rate filter has its own part number and top assembly drawing plus the sub-assembly drawings necessary to assemble an individual bit-rate filter. This method of documentation results in a greater number of drawings than possible alternate methods but does minimize parts selection during manufacturing.

Following is a list of the top assembly drawings for each bit-rate filter and the schematics.

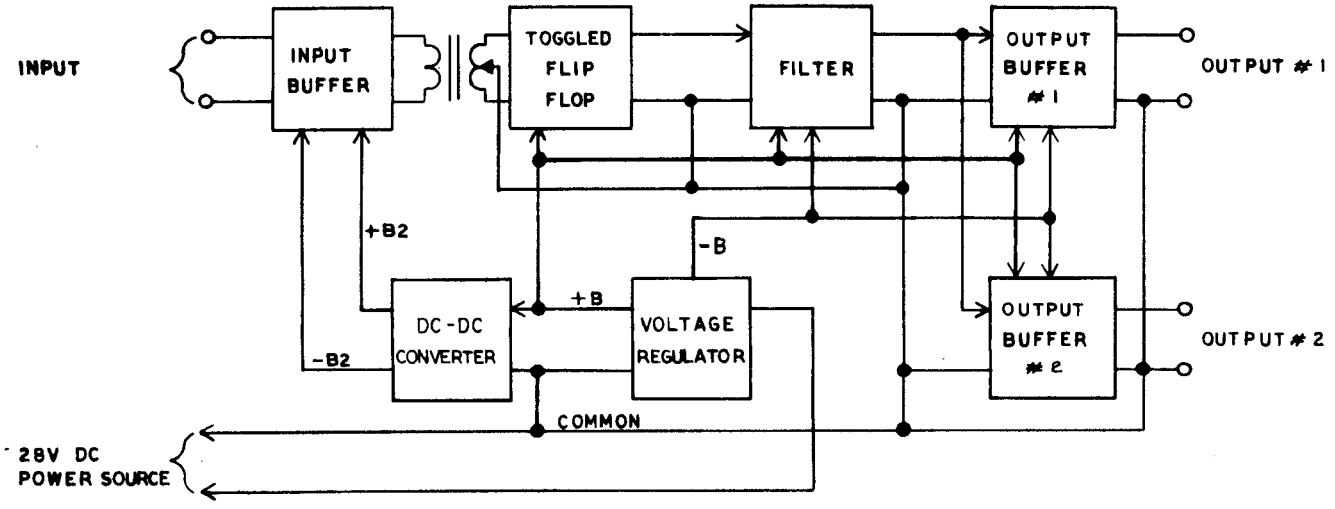
Title	Dwg. No.
Pre Modulation Filter Assembly 800 Bit/sec	1185001
Pre-Modulation Filter Assembly 1600 Bit/sec	1185019
Pre-Modulation Filter Assembly 3200 Bit/sec	1185023
Pre-Modulation Filter Assembly 6400 Bit/sec	1185027
Pre-Modulation Filter Assembly 12,800 Bit/sec	1185031
Pre-Modulation Filter Assembly 25,600 Bit/sec	1185035
Schematic Pre-Modulation Filter 800 Bit/sec	1185002
Schematic Pre-Modulation Filter 1600 Bit/sec	1185020
Schematic Pre-Modulation Filter 3200 Bit/sec	1185024

Title	Dwg. No.
Schematic Pre-Modulation Filter 6400 Bit/sec	1185028
Schematic Pre-Modulation Filter 12,800 Bit/sec	1185032
Schematic Pre-Modulation Filter 25,600 Bit/sec	1185036

5.0 TEST RESULTS

Complete test results are given for all units in the Qualification Test Report and the Pre-Modulation Test Data Sheets.

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVAL



NO. REQ'D.	ITEM NO	DESCRIPTION	MIL. SPEC.	MFR'S. PT. NO. / DRAWING NO.	REMARKS / MFR'S CODE

LIST OF MATERIALS

———	WO 1185
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES; TOLERANCES ON: FRACTIONS DECIMALS ANGLES
MATERIAL
HEAT TREATMENT
FINAL PROTECTIVE FINISH

DRAWN	JKL
DATE	21 APR 66
CHECKED	
DATE	
APPROVED	
DATE	
PROJ. ENG.	
DATE	

BLOCK DIAGRAM, PRE-MODULATION FILTER FIGURE 1

SCALE NONE
UNIT WT.

Space Craft Inc.

DWG. SIZE B

SCI-1185060

SHEET 1 OF 1

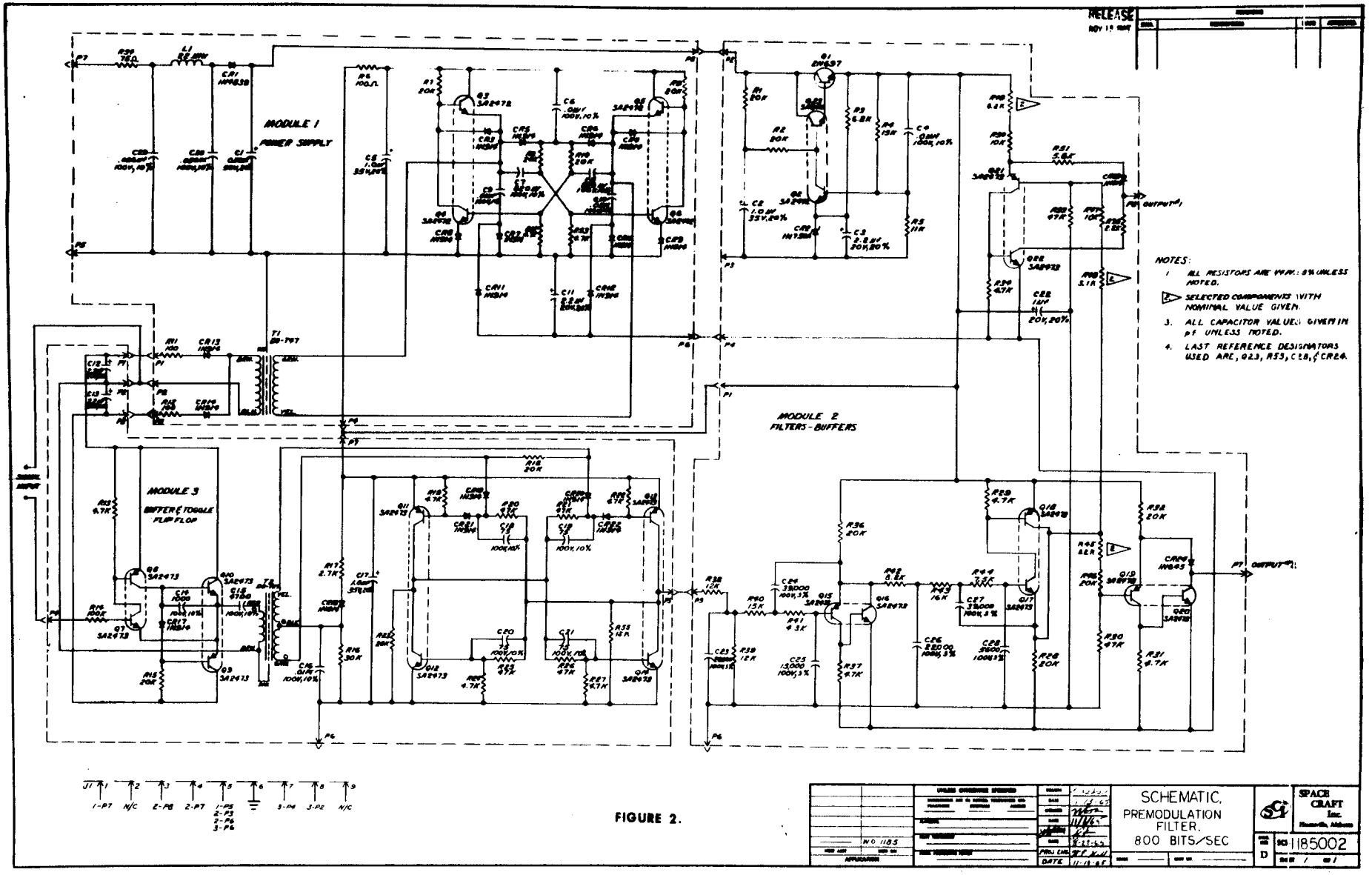

RELEASE
MODULE 1
POWER SUPPLY
MODULE 2
FILTERS - BUFFERS
MODULE 3
BUFFER & TOGGLE FLIP FLOP
NOTES:
1. ALL RESISTORS ARE ¼W, ±5% UNLESS NOTED.
2. SELECTED COMPONENTS WITH NOMINAL VALUE GIVEN.
3. ALL CAPACITOR VALUES GIVEN IN pf UNLESS NOTED.
4. LAST REFERENCE DESIGNATORS USED ARE, Q23, R53, C28, & CR24.
J1 1-P7 N/C 2-P8 2-P7 1-P5 2-P3 2-P6 3-P6 3-P4 3-P2 N/C
SCHEMATIC, PREMODULATION FILTER. 800 BITS/SEC
SPACE CRAFT Inc.
SCI 1185002
D

FIGURE 2.